

REMARKS

Applicants' representative thanks the Examiner for conducting the telephone interview on October 29, 2003. As discussed in the interview, most of Applicants claims recite specific systems and architectural arrangements. Claim 24, for example, recites "an arithmetic logic unit coupled to the at least one input buffer and the multiplication logic unit." Claim 24 similarly recites "a lighting unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit." The July 29 Office Action does not properly address these elements or their specific connections to other elements. And the applied references, *Peercy* (U.S. Patent no. 6,163,319) and *Parikh* (U.S. Patent no. 6,175,367), do not teach or render obvious such elements or connections. Applicants thus submit that this application is allowable over the applied references, whether considered individually or in combination.

Peercy is deficient for several reasons and is not subject to a proper combination with *Parikh*. For example, *Peercy* does not teach or suggest claim 24's "arithmetic logic unit" that is "coupled to the at least one input buffer and the multiplication logic unit." The portions of *Peercy* cited by the Office Action as teaching this "arithmetic logic unit" (col. 21, line 30 to col. 24, line 35 and fig. 9) are directed at a method for bump mapping in object space. *Peercy*'s Figure 9 is actually a flowchart rather than any type of architectural diagram, and this flow chart does not disclose any architectural details. In particular, neither the flowchart of Figure 9 nor any other portion of *Peercy* discloses the claimed "arithmetic logic unit" or its coupling to the "input buffer and the multiplication logic unit."

Claim 24 also recites a “lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit.” *Peercy* does not teach or render obvious such a “lighting logic unit.” Although *Peercy*’s Figure 10 illustrates a “lighting equation module” 450, this module is not the same as Applicants’ claimed “lighting logic unit,” which is coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit. *Peercy*’s “lighting equation module” 450 is not coupled to all three of these elements.

The combination of *Peercy* with the secondary reference, *Parikh*, does not remedy *Peercy*’s deficiencies. The Office Action only cites *Parikh* as teaching a “register unit” that is not taught by *Peercy*. *Parikh* does not disclose the claimed “arithmetic logic unit” or the “lighting logic unit,” and the Office Action does not even suggest that *Parikh* can do so. The combination of *Parikh* and *Peercy*, accordingly, can not render claim 24 obvious.

Those claims that depend from claim 24 are also allowable because they depend from claim 24. Several of these dependent claims, however, include independently allowable subject matter. Claim 25, for example, recites that the “multiplication logic unit has a feedback loop.” Neither *Peercy* nor *Parikh* teach or render obvious such a feedback loop.

The remaining independent and dependent claims are allowable for similar reasons. Independent claims 30, 34, 35, 40, and 41 all recite specific architectures that are not disclosed in *Peercy* or *Parikh*, whether taken individually or in combination. These claims, and the corresponding dependent claims, should be in condition for allowance.

CONCLUSION

Applicants respectfully submit that the claims as presented are distinguishable over the applied references. Because no other objections or rejections are outstanding, Applicants request an indication of allowability.

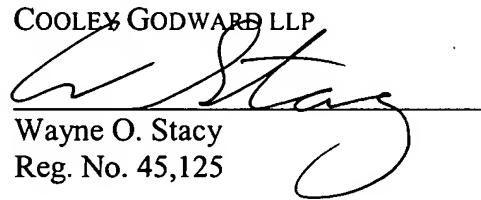
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